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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,547	02/19/2002	Hideya Akashi	520.41205X00	1476

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MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,547	AKASHI ET AL.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

2. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4, 5, 11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by BOLAND (U.S. Patent 5,872,972).

As to claim 1, BOLAND teaches a scheduling method for assigning a process (process) to be executed to one of a plurality of processors (processors) in a computer

system comprising the plurality of processors (processors), at least a part of the plurality of processors having a performance measuring means (via computing the headroom for each processor in order to determine the processor state) individually, each of the performance measuring means obtaining processor operation characteristics (idle and waiting on IO time) while executing a program of the processor (col. 5, lines 13-60; col. 4, line 63-67), the scheduling method comprising the steps of: when executing a process (process) by one of the processors (processor), obtaining the processor operation characteristics of the process by controlling the performance measuring means (via calculating the headroom for each processor); and selecting with priority a processor, to which each process is assigned, on the basis of the processor operation characteristics of each process that is being executed or can be executed in the computer (via selecting a processor to migrate processes or send available processes based on the operation characteristics) (col. 7, lines 14 – col. 8, line 13).

As to claim 11, BOLAND teaches a computer system having a plurality of processors (processors), wherein each of the processors has one or more performance measuring units (code) comprising a pair of a performance measuring data register for counting the number of times a specific event (idle event / waiting for I/O event) has taken place from among a plurality of events that have taken place in the processor (via the processor maintaining the sum of idle and waiting-on-IO time accumulated during a recent window of time) (col. 5, lines 13-60), and a performance measuring control register for indicating an event that should be measured by the performance measuring

data register (via using the times to determine the headroom by the scheduler) (col. 5, lines 13-60); and the performance measuring unit can obtain a change in the specific event in a time slice (window of time) by successively storing a value of the performance measuring data register in an area for performance measurement, which is provided in a memory of the computer system (via using the times to determine the headroom by the scheduler) (col. 5, lines 13-60).

As to claims 13 and 14, BOLAND teaches a scheduling method for assigning a process (process) to be executed to one of a plurality of processors (processors) in a computer system comprising the plurality of processors (processors), at least a part of the plurality of processors having a performance measuring means individually, each of the performance measuring means obtaining processor operation characteristics while executing a program of the processor (via computing the headroom for each processor in order to determine the processor state for the processor monitored idle time and waiting-on-I/O time) (col. 5, lines 13-60), the scheduling method comprising the steps of: when executing a process (process) by one of the processors, obtaining a ratio of the memory access wait time (waiting on IO time) to process execution time for the processes as the processor operation characteristics (headroom value) (col. 5, lines 13-60; col. 5, lines 2-12) and assigning a process of the highest ratio of the memory access wait time (process to steal) to a processor having the smallest memory access latency (via a processor with more headroom should steal processes from processor A until its headroom comes below the threshold to thereby improve cache memory utilization and

reduce memory and system bus traffic) (col. 5, lines 2-13; col. 8, lines 2-19). It would be inherent to the teachings of BOLAND that the selected processor has a larger capacity cache since the processor would not have increased wait time for retrieving information from a higher level memory (col. 3, line 63 – col. 4, line 13; col. 4, line 51 – col. 5, line 2).

As to claim 2, BOLAND teaches a ratio of memory access wait time to program execution time is used as the processor operation characteristics (via a processor with more headroom should steal processes from processor A until its headroom comes below the threshold to thereby improve cache memory utilization and reduce memory and system bus traffic, wherein the headroom is for example 5% or 20% of the total time elapsed in the window) (col. 5, lines 2-13; col. 8, lines 2-19).

As to claims 4 and 5, BOLAND teaches a ratio of memory access wait time to program execution time is used as the processor operation characteristics (via a processor with more headroom should steal processes from processor A until its headroom comes below the threshold to thereby improve cache memory utilization and reduce memory and system bus traffic, wherein the headroom is for example 5% or 20% of the total time elapsed in the window) (col. 5, lines 2-13; col. 8, lines 2-19). It would be inherent to the teachings of BOLAND that the selected processor has a larger capacity cache and smaller latency since the processor would not have increased wait

time for retrieving information from a higher level memory (col. 3, line 63 – col. 4, line 13; col. 4, line 51 – col. 5, line 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 6, 7, 10, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOLAND (U.S. Patent 5,872,972) in view of ABRAMSON (U.S. Patent 5,506,987).

As to claims 7 and 12, BOLAND teaches when executing a process (process) by one of the processors (processor), obtaining the processor operation characteristics of the process by controlling the performance measuring means (via calculating the headroom for each processor); and selecting with priority a processor, to which each process is assigned, on the basis of the processor operation characteristics of each process that is being executed or can be executed in the computer (via selecting a processor to migrate processes or send available processes based on the operation characteristics) (col. 7, lines 14 – col. 8, line 13). However, BOLAND does not teach the recording of processor characteristics such that the process is assigned to the recorded processor.

ABRAMSOM teaches scheduling processes on a symmetric multi-processing system based on monitoring characteristics wherein the processor characteristics are allow the process to execute with the same CPU (col. 2, lines 58-62; col. 9, lines 25-41). It would be obvious that the assigned processor would have to be stored as corresponding to the process in order for the process to be executed by the same CPU. Therefore, it would be obvious to one skilled in the art to combine the teachings of BOLAND with the teachings of ABRAMSOM so that allow the system to run high priority processes with the same CPU, i.e. they do not migrate (col. 2, lines 58-62).

As to claims 3, 6 and 10, BOLAND substantially discloses the invention above. However, BOLAND does not teach a memory access size is used as the processor operation characteristics wherein processes are assigned with priority on the basis of the memory access size of the process so that a total memory access size of the processes doe not exceed memory access performance on the node and obtaining a change in a memory access size of each process by controlling the performance measuring means.

ABRAMSOM teaches a method for scheduling processes on a symmetric multi-processing system based on monitoring characteristics wherein a memory access size (memory usage) is used as the processor operation characteristics wherein processes are assigned with priority on the basis of the memory access size (memory usage thereby sorting processes as large or small processes) of the process so that a total memory access size of the processes does not exceed memory access performance on

the node (via load balancing the large and small processes based on processor capacity) and obtaining a change in a memory access size of each process by controlling the performance measuring means (via migrating the processes to other nodes to balance the load) (col. 6, lines 40-65; col. 7, lines 3-45; col. 5, lines 10-14). Therefore, it would be obvious to one skilled in the art to combine the teachings of BOLAND with the teachings of ABRAMSOM in order to maintain process-to-CPU affinity without introducing excessive idle time (col. 2, lines 10-13).

As to claim 15, BOLAND teaches obtaining memory access throughput of each process being executed as the processor operation characteristics (via monitoring the idle / waiting times of the processor to the process); and assigning each process to the processor so that a total memory access throughput of one or more processes, which are assigned to each node, does not exceed memory access throughput performance of the node (via assigning the process to the stealing processor that can execute the process based on the headroom) (col. 5, lines 1-60; col. 4, lines 51-67). However, BOLAND does not teach the computer system having a plurality of nodes.

ABRAMSON teaches a scheduling computer system that has a plurality of nodes (CPU subsystems), each of which is a processor configuration comprising one or more processors (processors), the node sharing the same memory (global memory) and being controlled by the same operating system (col. 3, line 40 – col. 4, line 50) and capable of assigning / migrating a process to another processor based on operation characteristics (memory usage) (abstract). Therefore, it would be obvious to combine

the teachings of BOLAND with the teachings of ABRAMSON to maintain process-to-CPU affinity without introducing excessive idle time (col. 2, lines 10-13).

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOLAND (U.S. Patent 5,872,972).

As to claims 8 and 9, BOLAND teaches the memory access characteristics are obtained and calculated by a time slice (window of time) such that processes are reassigned based on the following conditions: (1) The non-affinitized process has no affinity to another processor, e.g. a new process; (2) The age of the non-affinitized process is greater than a predetermined "steal-age" threshold; or (3) The processor to which the non-affinitized process is affinitized is in a "no-headroom" state wherein if it is detected that there is a memory access wait ratio in a time slice (window of time) to decrease to a level below than a threshold value (headroom is above or below a threshold) determined by a scheduling function on the basis of memory access characteristics, the process is migrated (col. 5, lines 1-60; col. 6, lines 23-34; col. 7, line 66 – col. 8, line 19). However, BOLAND does not allude to assigning a processor time to the process and changing the processor time to the process. BOLAND does teach that process are executed based on their priority and are assigned or migrated to the least loaded processor (fig. 3 and 4). Therefore, it would be obvious to the teachings of BOLAND that processes are assigned processor time in order to execute and that the processor time is incremented and decremented based on the amount of higher priority processes on the processor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 27, 2005

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER